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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,312	06/28/2000	Andrew J. Wright	0325.00353	6231

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EXAMINER
CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,312	WRIGHT, ANDREW J.	
	Examiner	Art Unit	
	James H. Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Sako (US PAT No. 6,194,914).

Regarding claim 1, Fig. 13 of Sako discloses an apparatus (TU) comprising a polarity switch (col. 19, line 56 - col. 20 line 46) comprising a number of transmission

gates (M1 and M3, M4 and M2) where an output (U) of the polarity switch selectably presents either a signal that varies in response to a control signal (c) or a predetermined logic level that is independent of the control signal (when a and b are a logic low, the output U stays the predetermined value of a logic low, when a and b are a logic high, the output U stays the predetermined value of a logic high, when a and b are a logic low and a logic high respectively, the output U varies according to the logic value of the complement of c, and when the a and b are a logic high and a logic low respectively, the output U varies according to the logic value of c).

Regarding claim 2, Fig. 13 of Sako discloses the apparatus according to claim 1 where the number of transmission gate is two (the first one comprising M1 and M3 and the second one comprising M4 and M2).

Regarding claim 3, Fig. 13 of Sako discloses the apparatus according to claim 1 where the output signal is selected in response to a first configuration signal and a second configuration signal (a and b as discussed in claim 1).

Regarding claim 4, Fig. 13 of Sako discloses the apparatus according to claim 1 and Figs. 11-12 and 18 of Sako further discloses a first storage element (FF1) connected to an input of a first transmission gate (see col. 29, line 62- col. 30, line 35), and a second storage element (FF2) connected to an input of a second transmission

gate (flip-flops are commonly used by logic circuits in a plurality of programmable logic blocks).

Regarding claim 5, Fig. 13 of Sako discloses the apparatus according to claim 1 where the control signal is an input term (signal c is an input term for the output U).

Regarding claims 6 and 18, Figs, 11-12, 13 and 18 of Sako discloses an apparatus (TU in Fig. 13) and the method for providing a product term input of programmable logic device comprising a first circuit (M1 and M3) configured to present a first stored value (the inputs a, b are the outputs of another logic block having flip-flops shown in Fig. 11, 12 and 18) to an input node (the output node U is an input node for the next stage of programmable logic block) in response to a first state of a control signal (c), and a second circuit (M4 and M2) configured to present a second stored value (the inputs a, b, c are the outputs of another logic block having flip-flops shown in Fig. 11, 12 and 18) to the input node in response to a second state of the control signal (when a and b are a logic low, the output U stays the predetermined value of a logic low, when a and b are a logic high, the output U stays the predetermined value of a logic high, when a and b are a logic low and a logic high respectively, the output U varies according to the logic value of the complement of c, and when the a and b are a logic high and a logic low respectively, the output U varies according to the logic value of c).

Regarding claim 7, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 6, where the first and second circuits comprise transmission gates(M1 and M3, M4 and M2 in Fig. 13).

Regarding claim 8, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 7 where the transmission gates comprises a CMOS transistor pair (M1 and M3, M4 and M2 in Fig. 13).

Regarding claim 9, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 6 where the first and second circuits comprise a first and second storage (FF1 and FF2 in Fig. 11 and 12), respectively.

Regarding claim 10, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 9, the first and second storage elements contain the same or different data (data in FF1 and FF2 depends on the previous stage of the programmable logic circuit).

Regarding claim 11, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 10 where data comprises configuration data (the output of FF1 and FF2 are configuration data for the next stage).

Regarding claim 12, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 9, where the first and second storage elements are configured to source or sink a current (it is inherent that when the output of FF1 and FF2 is high, FF1 and FF2 source a current while they sink a current when the output of FF1 and FF2 is low).

Regarding claim 13, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 6, where the apparatus comprises a product term input circuit of a programmable logic device (ABSTRACT).

Regarding claim 14, Figs, 11-12, 13 and 18 of Sako discloses an AND plane of a programmable logic device comprising one or more apparatus according to claim 6 (col. 49, lines 36-54).

Regarding claims 15 and 19, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 6 and the method according to claim 18 where the control signal comprises an input term (c is an input term for the pass transistor logic switch TU in Fig. 13).

Regarding claims 16-17 and 20, Figs, 11-12, 13 and 18 of Sako discloses the apparatus according to claim 15 and the method according to claim 18 where the apparatus is programmed to present the input term, a digital complement of the input

term or a logic level to the input node (when a and b are a logic low, the output U stays the predetermined value of a logic low, when a and b are a logic high, the output U stays the predetermined value of a logic high, when a and b are a logic low and a logic high respectively, the output U varies according to the logic value of the complement of c, and when the a and b are a logic high and a logic low respectively, the output U varies according to the logic value of c).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Igura (US PAT No. 5,687,107) discloses an exclusive OR gate, an inverted type selector, and adders.

Inoue et al. (US PAT No. 5,233,233) discloses a multiplexer for use in a full adder having different gate delays.

Shiotani (JP 61173518A) discloses a detecting circuit for signal brake.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-0142 for regular communications and 703-308-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

James Cho

January 27, 2003